CS 6070 : ARCHITECTURE OF COMPUTERS

Semester Hours:	3.0	*Contact Hours:* 3
Coordinator:	Jong Kwan "Jake" Lee	
Text:	TBD	
Author:	TBD	
Year:	TBD	

SPECIFIC COURSE INFORMATION

Catalog Description:

Architectures of modern computing systems. Techniques for high-speed computation: pipelining, vector processing, array processors. General purpose parallel architectures: SIMD, MIMD and data flow systems and their memory organizations and processor communication. Prerequisites: Full Admission to MS in CS program or consent of department.

Course type: **ELECTIVE**

SPECIFIC COURSE GOALS

- I understand the quantitative principles (e.g. taking advantage of parallelism, exploring principle of locality, losing on the common case) of computer design.
- I understand the pipelining works on a modern CPU.
- I can explore instruction level parallelisms (e.g. loop unrolling, scheduling, branch prediction) in RISC/MIPS instruction sets.
- I understand how vector processing works.
- I understand cache structure and its relevant concepts (e.g. cache performance evaluation, replacement policies).

LIST OF TOPICS COVERED

- Introduction to Technology and Architecture*
  - Impact of technology on computer architecture
  - Evolution of computer architecture
- Associative Memory (CAM)
  - Hardware concepts of CAM
  - Lewin's O(n) sorting algorithm
- Cache Memory*
  - Basic cache structure
  - Set associative caches

    - Evaluating Cache performances
    - Determining Cache parameters
    - Replacement Policies
    - Implementing LRU replacement policies
    - Detail example of a cache memory system
- Virtual Memory*
    - Basic virtual memory structure
    - Translation lookaside buffer
    - Segment tables
    - Replacement algorithms
    - Detail example of a virtual memory system
- Pipeline Techniques*
    - Principles of Pipelined computers
    - Evaluating performance of pipelined computers
    - Reservation tables and collision vectors
    - Maximizing pipeline performance
    - Conditional branches in pipelined computers
    - Internal forwarding and deferred instructions
- Reconfigurable computer architectures
    - Reconfigurable busses
    - Addition in time O(1)
- Multiprocessors
    - Flynn's classification of multiprocessors
    - Vector computers*
        - Numerical algorithms on a vector computer
        - Pipelining in vector computers
        - Examples of vector computers
    - Multiprocessor interconnections*
    - General purpose multiprocessors, e.g. RP-1, HEP
    - Data flow computers
- RISC Computers
    - Pipelined structure of the CPU
    - RISC characteristics
    - Detail example of a RISC computer

*This topic is core material to be covered every time the course is taught.